

REMARKS

Applicants thank the Examiner for indicating that claims 4-13 and 15-17 contain allowable subject matter.

I. Introduction

Claims 1-17 are pending in the above application.

Claims 1-3 and 14 stand rejected under 35 U.S.C. §102.

Claims 4-13, 16 and 17 stand allowed.

Claims 15 is indicated as containing allowable subject matter. Prior to the amendment herein, claim 15 was dependent upon rejected claim 1.

Claims 18 and 19 have been cancelled without prejudice or disclaimer.

Claims 1, 4, 8 and 12 are the independent claims.

II. Amendment

Claims 1, 14 and 15 have been amended. Claims 14 and 15 are now in independent form to include all of the limitations of original claim 1. Claim 14 has been further amended.

No new matter has been added.

III. Prior Art Rejections

Claims 1-3 and 14 stand rejected under 35 U.S.C. §102 as being anticipated by Matsumoto et al. (U.S. Pat. 6,455,894) (hereafter "Matsumoto") as set forth on pages 2-3 of the Office Action.

Anticipation under 35 U.S.C. § 102 requires that each and every element of the claim be disclosed in a prior art reference as arranged in the claim. See, C.R. Bard, Inc. v. M3 Sys., Inc., 157 F.3d 1340, 1349, 48 U.S.P.Q.2D (BNA) 1225 (Fed. Cir. 1998); and Connell v. Sears, Roebuck & Co., 220 USPQ 193, 198 (Fed. Cir. 1983).

A. Claims 1-3 Are Not Anticipated

Claim 1, as amended, recites, *inter alia*:

wherein the dummy diffused layer has its surface covered with an anti-silicidation film at least partially, on which no gate electrode is provided.

Matsumoto does not disclose or suggest a semiconductor device having a dummy diffused layer which has its surface covered with an anti-silicidation film at least partially, on which no gate electrode is provided, as required by amended claim 1. The Office action cites to Figure 9 in Matsumoto as disclosing a film 4c which partially covers a dummy diffused layer. However, as shown in Figure 9 of Matsumoto, the film 4c is merely a dummy gate insulating film, on which a dummy gate electrode 7c is provided. Matsumoto does not disclose or suggest a semiconductor device having a dummy diffused layer which has its surface covered with an anti-silicidation film at least partially, on which no gate electrode is provided, as required by amended claim 1. Matsumoto does not disclose each and every element of amended claim 1 as arranged in amended claim 1. Hence, Matsumoto does not anticipate amended claim 1, nor claims 2-3, which depend on amended claim 1 and contain all the limitations therein.

B. Claim 14 Is Not Anticipated

Claim 14, as amended, recites, *inter alia*:

wherein the dummy diffused layer has its surface covered with an anti-silicidation film at least partially, and

wherein the dummy diffused layer is located between an analog circuit block and a digital circuit block.

Matsumoto does not disclose or suggest a semiconductor device in which the dummy diffused layer has its surface covered with an anti-silicidation film at least partially, and the dummy diffused layer is located between an analog circuit block and a digital circuit block, as required by amended claim 14. Matsumoto does not disclose each and every element of amended claim 14 as arranged in amended claim 14. Hence, Matsumoto does not anticipate amended claim 14.

IV. Conclusion

Accordingly, it is urged that the application is in condition for allowance, an indication of which is respectfully solicited.

If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

Respectfully submitted,

McDERMOTT, WILL & EMERY

Date: April 3, 2003

By:



Lawrence T. Cullen
Registration No.: 44,489

600 13th Street, N.W., Suite 1200
Washington, D.C. 20006-3096
Telephone: (202) 756-8000
Facsimile: (202) 756-8087